Space Vector Pulse Width Modulation Schemes for Two-Level Voltage Source Inverter

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***Abstract*—Space Vector Pulse Width Modulation (SVPWM) method is an advanced, computation intensive PWM method and possibly the best among all the PWM techniques for variable frequency drive applications. The SVPWM is an alternative method for the determination of switching pulse width and their position. The major advantage of SVPWM stem from the fact that, there is a degree of freedom of space vector placement in a switching cycle. This feature improves the harmonic performance of this method. This method has been finding widespread application in recent years because of the easier digital realization and better dc bus utilization. In this paper, three SVPWM schemes, called 7-segment space vector modulation (SVM), 7-segment SVM with even-order harmonic elimination and 5-segment (discontinuous) SVM are studied in detail. The theoretical analysis, design, switching sequence and SIMULINK implementation of these three SVM schemes is presented in step-by-step manner.**

***Index Terms*—SVPWM, 7-Segment SVM, 5-Segment SVM, Two -Level Inverter, SIMULINK**

I. INTRODUCTION

In recent years, Space Vector Pulse Width Modulation (SVPWM) technology gradually obtains widespread applications in the power electronics and the electrical drives. It reduces motor axis pulsation and current waveform distortion, moreover, its DC voltage utilization ratio has been enhanced very much which is 70.7% of the DC link voltage (compared to the conventional Sine-Pulse width Modulation's 61.2%), in the linear modulation range and it is also easier to realize digitally [3].

There are three different algorithms for using SVPWM to modulate the inverter. Many SVPWM schemes have been investigated extensively in the literature [5-7]. The goal in each modulation strategy is to lower the switching losses, maximize the bus utilization, reduce harmonic content and still achieve precise control. So, the performance of a SVPWM scheme is usually judged based on the following criteria: total harmonic distortion (THD) of the output voltages, switching losses of the inverter and the maximum output voltage.

In this paper three Space Vector Modulation (SVM) schemes called 7-segment space vector modulation (SVM), 7-segment SVM with even-order harmonic elimination and 5-segment (discontinuous) SVM are studied in detail and SIMULINK implementation of these three SVM techniques is presented.

II. PRINCIPLES OF SVPWM

SVPWM is based on the fact that there are only two independent variables in a three-phase voltage system. We can use orthogonal coordinates to represent the 3-phase voltage in the phasor diagram. A three-phase voltage vector may be represented as

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} V_{A0} \\ V_{B0} \\ V_{C0} \end{bmatrix} \quad (1)$$

In the SVPWM scheme, the three phase output voltage is represented by a reference vector, which, rotates at an angular speed of $\omega = 2\Pi f$. The task of SVM is to use the combinations of switching states to approximate the locus of V_{ref}, the eight possible switching states of the inverter are represented as two null vector vectors and six active vectors as listed in the Table 1.

TABLE I. SWITCHING STATES OF THE TWO LEVEL INVERTER

Space vector	Switching State	'On' Switches
Zero Vector	V_7	1,3,5
	V_0	4,6,2
Active vector	V_1	4,6,5
	V_2	4,3,2
	V_3	4,3,5
	V_4	1,6,2
	V_5	1,6,5
	V_6	1,3,2

These vectors (V_1~V_6) can be used to frame the vector plane, which is illustrated in Fig: 1. The rotating reference vector can be approximated in each switching cycle by switching between the adjacent active vectors and the zero vectors. In order to maintain the effective switching frequency at a minimal value, the sequence of the toggling between these vectors is organized in such a way that only one leg is affected in every step. For a given magnitude and position V_{ref}, can be synthesized by three nearby stationary vectors, based on which, the switching states of the inverter can be selected and gate signals for the active switches can be generated. When V_{ref}, passes through sectors one by one, different sets

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of switches will be turned on and off .As a result, when V_{ref}, rotates one revolution in space, the inverter output voltage varies one cycle over time.

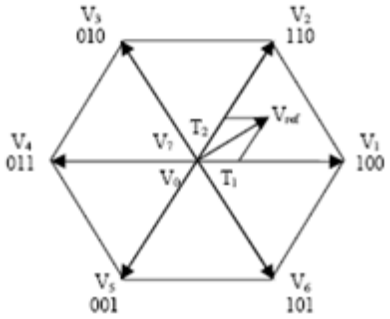

Fig.1. Switching vectors hexagon

Three stationary vectors can synthesize the reference V_{ref}. The dwell time for the stationary vectors essentially represents the duty-cycle time (on-state or off-state time) of the chosen switches during a sampling period Ts of the modulation scheme. The dwell time calculation is based on 'volt-second balancing' principle, that is, the product of the reference voltage V_{ref} and sampling period Ts equals the sum of the voltage multiplied by the time interval of chosen space vectors. For example, when V_{ref} falls into sector I as shown in Fig: 2, it can be synthesized by V_1, V_2 and V_0.The volt second balance equation is

$$\begin{aligned} V_{ref}T_s &= V_1T_0 + V_2T_b + V_0T_0 \\ T_S &= T_a + T_b + T_c \end{aligned} \tag{2}$$

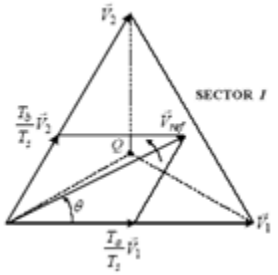

Fig.2. V_{ref} synthesized by V_1, V_2 and V_0

For linear modulation range, the dwell times can be calculated as:

$$\begin{aligned} T_a &= \frac{\sqrt{3}T_sV_{ref}}{V_d}\sin\left(\frac{\pi}{3}-\theta\right) \\ T_b &= \frac{\sqrt{3}T_sV_{ref}}{V_d}\sin(\theta), 0 \le \theta \le \frac{\pi}{3} \\ T_0 &= T_s - T_a - T_b \end{aligned} \tag{3}$$

II. 7 SEGMENT SPACE VECTRO MODULATION

The sector judgment and application time of active vector for all SVM strategies are the same. The choice of the null vector determines the SVM scheme. There are a few options: the null vector V_0 only, the null vector V_7 only, or a combination of the null vectors. A popular SVM technique is to alternate the null vector in each cycle and to reverse the sequence after each null vector. This will be referred to as the symmetric 7-segment technique. Fig. 3 shows conventional 7-segment switching sequences of sector I. It is shown that the sequence V_0-V_1-V_2-V_0 is used in the first $T_s/2$, and the sequence V_0-V_2-V_2-V_0 is used in the second $T_s/2$. The sequences are symmetrical. The switching frequency is the same as sampling frequency of the inverter.

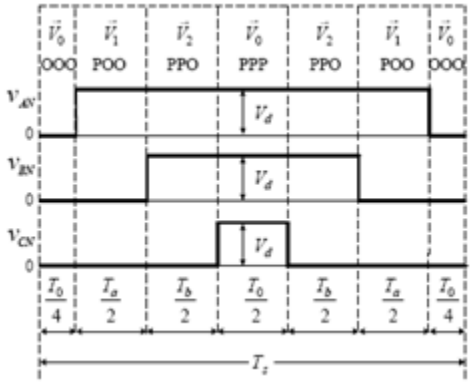

Fig.3. 7-Segment Switching Sequence for V_{ref} in sector I

The SIMULINK Implementation of the system has been carried out in the following sequence:

- Calculation of 3 phase voltages (MATLAB F_{cn} is used)
- Calculation of V_{alpha} and V_{bheta} (3 phase to 2 phase transformation block is used)
- Calculation V_{ref} and alpha (Polar to Rectangle block is used. The inputs to this block are V_{alpha} and V_{bheta} and outputs of this block are Vref and alpha.)
- Calculation of T_a, T_b, T_0 (Sub-system is shown in Fig.9)
- Calculation of sector value
- Calculation cumulative sum of T_a, T_b, T_0 (Sub-system is shown in Fig. 10)
- Calculation of T_n (Sub-system is shown in Fig. 11)
- Determination of switching states (look-up table is used
- Realization of switching states (multi-port switch is used)
- Derivation of 6 individual gate pulses to two level inverter

IV. 7 SEGMENT SVM WITH EVEN ORDER HARMONIC ELIMINATION

From the results of 7 segment SVM, it is clear that, the line-to-line voltage waveform contains even order harmonics. Since, most IEEE standards have more stringent requirements on even-order harmonics than odd-order harmonics; this section presents a modified SVM scheme with even-order harmonic elimination. To investigate the mechanism of even order harmonic elimination two switching sequences for the V_{ref} falls into sector IV are shown in Fig: 4. & Fig: 5. Space vector diagram is shown in Fig: 6.

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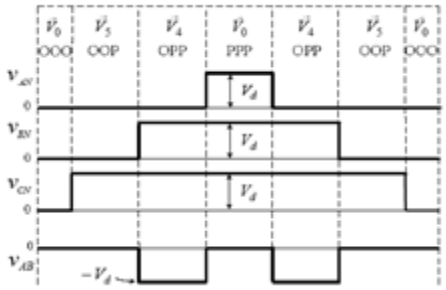

Fig.4. Type A Switching Sequence for V_{ref} in sector IV [start and ends with (0,0,0)]

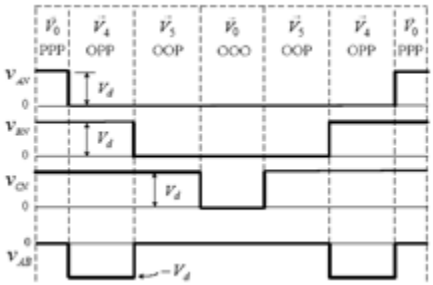

Fig.5. Type B Switching Sequence for V_{ref} in sector IV [start and ends with (P,P,P)]

To make the three-phase line-to-line voltage half-wave symmetrical, Type-A and Type-B switching sequences can be alternatively used. In addition, each sector in the space vector diagram is divided into two regions as shown in Fig. 6. Type-A sequence is used in the non-shaded regions, while type-B sequence is employed in the shaded regions.

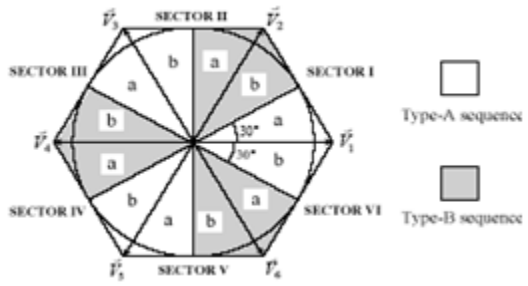

Fig.6. Space vector diagram for even order harmonic elimination

The SIMULINK Implementation of the system has been carried out in the following sequence:

- Calculation of 3 phase voltages (same as in the 7 segment model)
- Calculation of V_{alpha} and V_{bheta} (same as in the 7 segment model)
- Calculation V_{ref} and alpha (same as in the 7 segment model)
- Calculation of T_a, T_b, T_0 (same as in the 7 segment model)
- Calculation of sector value (This step is different from previous model. Here 12 sectors are calculated each with 30°)
- Calculation cumulative sum of T_a, T_b, T_0 (same as in the 7 segment model)
- Calculation of T_n (same as in the 7 segment model)
- Determination of switching states (look-up table is used)
- Realization of switching states (same as in the 7 segment model)
- Derivation of 6 individual gate pulses to two level inverter

V. Five segment SVM

The switching sequence design is not unique for a given set of stationary vectors and dwell times. Fig: 7 shows two five-segment switching sequences and generated inverter terminal voltages for V_{ref} in sector I. For type-A sequence, the zero switching sate [OOO] is assigned for V_0 while type-B sequence utilizes [PPP] for V_0.

In the five-segment sequence, one of the three inverter output terminals is clamped to either the positive or negative dc bus without any switching's during the sampling period Ts. Furthermore, the switching sequence can be arranged such that the switching in an inverter leg is continuously suppressed for a period of 2*pi/3 per cycle of the fundamental frequency.

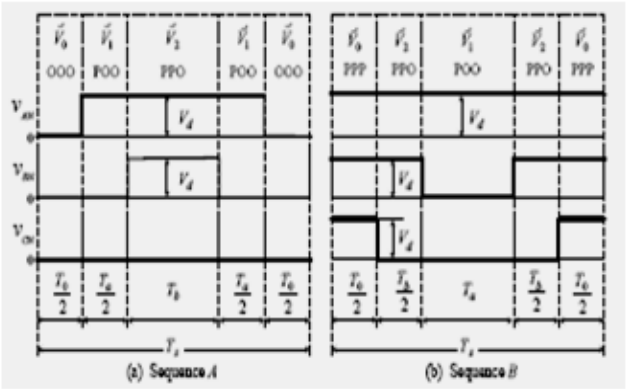

Fig.7. Five Segment switching sequence

The SIMULINK Implementation of the system has been carried out in the following sequence

- Calculation of 3 phase voltages (same as in the 7 segment model)
- Calculation of V_{alpha} and V_{bheta} (same as in the 7 segment model)
- Calculation V_{ref} and alpha (same as in the 7 segment model)
- Calculation of T_a, T_b, T_0 (same as in the 7 segment model)
- Calculation of sector value (same as in the 7 segment model)
- Calculation cumulative sum of T_a, T_b, T_0 (Sub-system is shown in Fig.14)
- Calculation of T_n (Sub-system is shown in Fig.15)
- Determination of switching states (look-up table is used)
- Realization of switching states (different from 7 segment model)
- Derivation of 6 individual gate pulses to two level inverter

VI. Matlab/simulink models of three SVM schemes

This section details the step-by-step development of MATLAB/SIMULINK models of the three SVM schemes.

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A. Simulink model of 7-Segment SVM

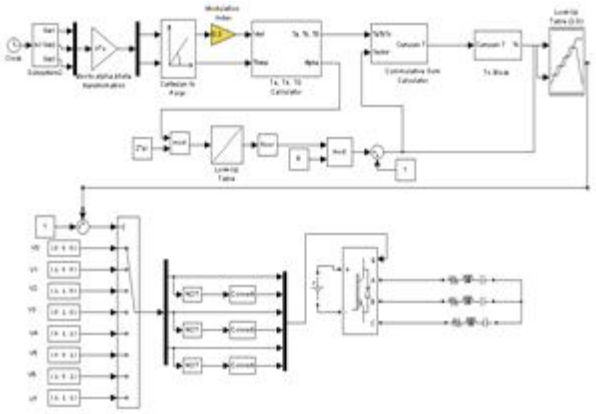

Fig.8. SIMULINK model of 7-Segment SVM

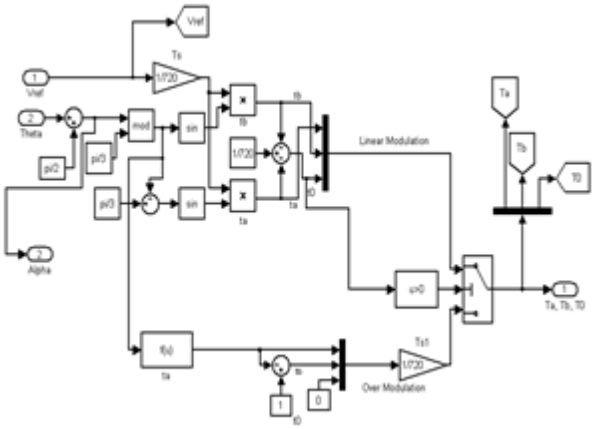

Fig.9. SIMULINK model of Ta, T_b, T_0 calculator

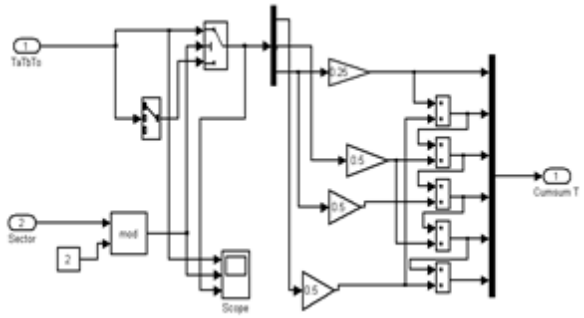

Fig.10. SIMULINK model of cumulative some calculator

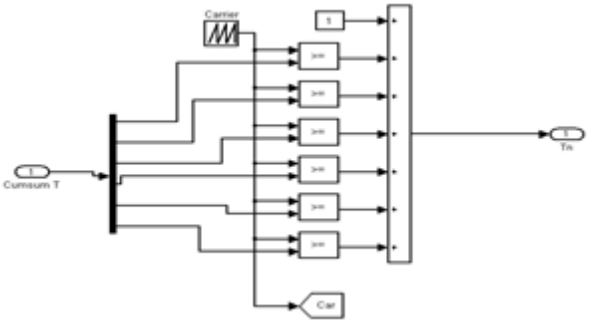

Fig.11. SIMULINK model of T_n block

B. Simulink model of 7-Segment SVM with even order harmonic elimination

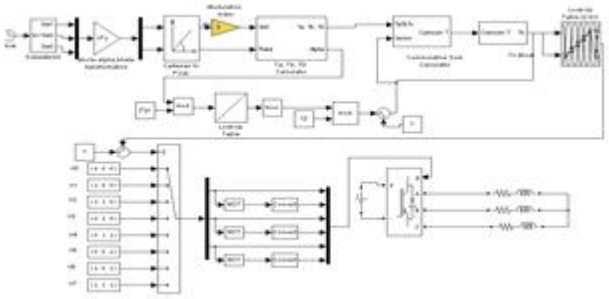

Fig.12. SIMULINK model of 7-Segment SVM with even order harmonic elimination

C. Simulink model of 5-Segment SVM

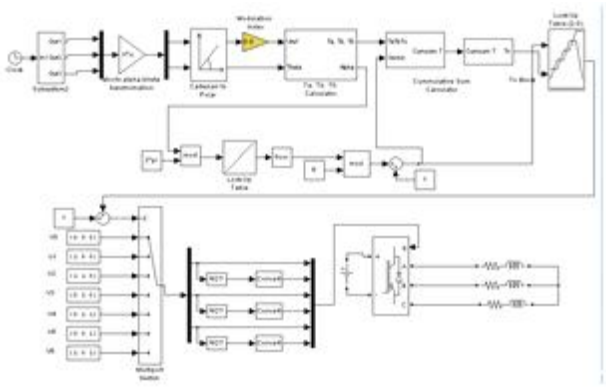

Fig.13. SIMULINK model of 5-Segment SVM

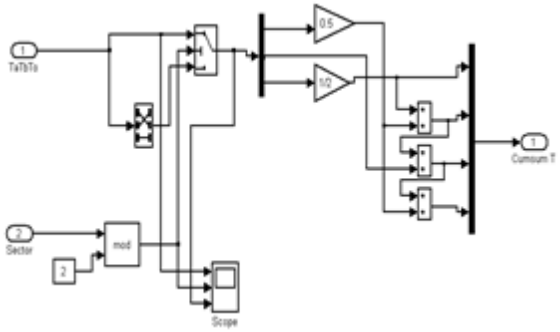

Fig.14. SIMULINK model of Cumulative sum calculator for 5-Segment SVM

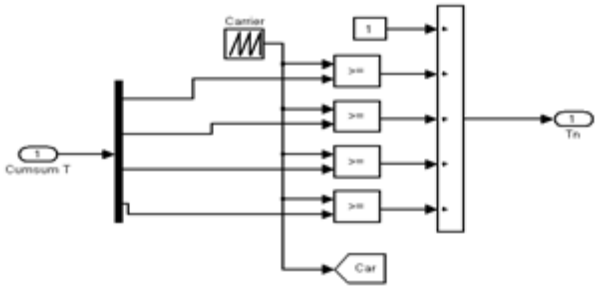

Fig.15. SIMULINK model of T_n block for 5-Segment SVM

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VII. Simulation results

Simulink models for the three SVM schemes were built respectively and the models were run according to the following data: DC Link Voltage V_d=5883 V, output line voltage line voltage frequency=60Hz, R=16.4Ω, L=14.2 mH. The simulation results were presented for m_a=0.8, f_1=60 Hz, and T_s=1/720 sec. for all the three schemes.

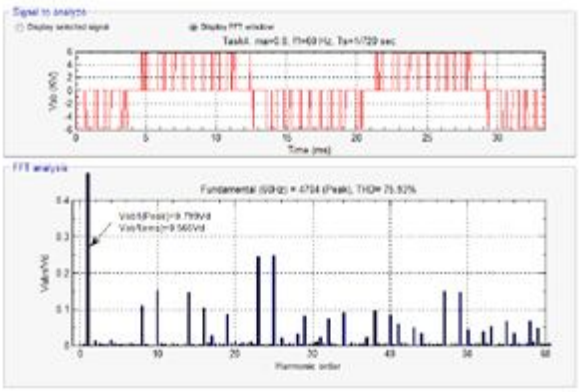

Fig. 16. Waveform and FFT analysis of V_{ab} for m_a=0.8, f_1=60 Hz, and T_s=1/720 sec 7-segment svm

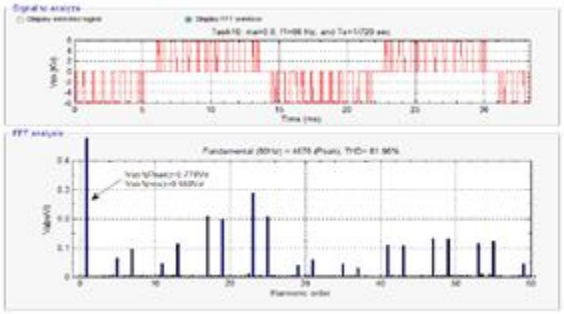

Fig. 17. Waveform and FFT analysis of V_{ab} for m_a=0.8, f_1=60 Hz, and T_s=1/720 sec 7-segment SVM with even order harmonic elimination

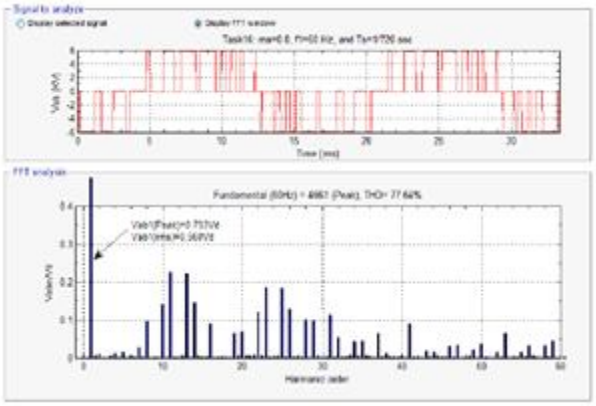

Fig. 18. Waveform and FFT analysis of V_{ab} for m_a=0.8, f_1=60 Hz, and T_s=1/720 sec 5-segment SVM

VIII. Conclusions

SVM is a popular choice in the inverter control. Three SVM schemes are presented and analyzed through simulation. The comparison study shows that all the three SVM schemes can obtain the same output voltage in linear modulation region. It was observed from the harmonic spectrum of three schemes, the 7-segment SVM scheme performs better in terms of THD of the output line voltage. It is also observed that the THD of the 5-segment SVM lies between the THD of 7-segment SVM and &7-segment SVM with even order harmonic elimination.

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